Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently Amended) An information processing apparatus as claimed in claim 18,

wherein said processing device comprises an external bus controller for preventing non-encrypted sensitive information from being output onto said bus.

3. (Original) An information processing apparatus as claimed in claim 2;

wherein information not requiring encryption is output onto said bus through said external bus controller.

4. (Currently Amended) An information processing apparatus as claimed in claim 18,

wherein a memory device is provided for storing information encrypted by said processing device.

5. (Currently Amended) An information processing apparatus as claimed in claim 18,

wherein said processing device comprises means for decrypting encrypted information at an information write operation.

6. (Original) An information processing apparatus as claimed in claim 5,

wherein said information processing apparatus is connected to a different information processing apparatus through a network, and

wherein said information processing apparatus decrypts encrypted information which is received from said different information processing apparatus.

7. (Currently Amended) An information processing apparatus as claimed in claim 1<u>8</u>,

wherein a plurality of said processing devices are provided, and cryptographic processing is carried out in each of said processing devices.

8. (Currently Amended) An information processing apparatus as claimed in claim 1<u>8</u>,

wherein said processing device comprises means for receiving an encrypted program and for carrying out decryption thereof.

9-13. (Canceled)

14. (Currently Amended) An information processing apparatus as claimed in claim 18,

wherein said abnormality is a disassembly or removal of a case or housing of said processing device.

15. (Currently Amended) An information processing apparatus as claimed in claim 18,

wherein said first key information is a random number, and

wherein said generator generates said random number based on a signal outputted from a constant voltage diode.

16. (Currently Amended) An information processing apparatus ~~as claimed in claim 9~~ including,

a processing device for performing predetermined processing of information, and

a bus for interconnecting said processing device and other component devices of said information processing apparatus,

wherein said processing device is integrated on a single semiconductor chip, internally generates first key information and second key information, internally encrypts sensitive information inputted from said bus with said generated second key information, internally encrypts said generated second key information with said generated first key information, and outputs said encrypted sensitive information and

said encrypted second key information to said bus without outputting said first key information used for encrypting said second key information to said bus,

wherein said processing device newly generates different second key information each time sensitive information inputted from said bus is encrypted,

wherein said first key information is common to a plurality of said second key information, and

wherein said processing device deletes said first key information in said single semiconductor chip if an abnormality is detected,

wherein said processing device comprises:

a microprocessor for carrying out said predetermined processing;

a generator for generating said first key information;

a cryptographic algorithm memory device for storing an algorithm for information cryptographic processing;

a volatile memory device for storing said generated first key information;

a cryptographic processing device for carrying out cryptographic processing with said algorithm; and

a microprocessor bus for interconnecting said microprocessor, said generator, said cryptographic algorithm memory device, said volatile memory device and said cryptographic processing device,

wherein a power supply to said volatile memory is stopped so as to delete said first key information in said single semiconductor chip if said abnormality is detected, and

wherein said processing device voids a control signal to said volatile memory until an internal logical block in said processing device is finished initializing.

17. (Canceled)

18. (Currently Amended) An information processing apparatus ~~as claimed in claim 17,~~including,

a processing device for performing predetermined processing of information, and

a bus for interconnecting said processing device and other component devices of said information processing apparatus,

wherein said processing device is integrated on a single semiconductor chip, internally generates first key information and second key information, internally encrypts sensitive information inputted from said bus with said generated second key information, internally encrypts said generated second key information with said generated first key information, and outputs said encrypted sensitive information and said encrypted second key information to said bus without outputting said first key information used for encrypting said second key information to said bus,

wherein said processing device newly generates different second key information each time sensitive information inputted from said bus is encrypted,

wherein said first key information is common to a plurality of said second key information,

wherein said processing device deletes said first key information in said single semiconductor chip if an abnormality is detected,

wherein said processing device comprises a battery backed first RAM for storing said generated first key information and a second RAM for storing said generated second key information, said second RAM including a working area, and

wherein said processing device voids a control signal to said battery backed first RAM until an internal logical block in said processing device is finished initializing.

19. (Canceled)